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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,432	12/15/2000	Jun Souk Joung	HI-023	8762

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EXAMINER	
DELGADO, MICHAEL A	
ART UNIT	**PAPER NUMBER**
2144	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/736,432	JOUNG, JUN SOUK	
	Examiner	Art Unit	
	Michael S. A. Delgado	2144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10,11,15-20 and 25-27* is/are rejected.

7)☒ Claim(s) *6-9,12-14 and 21-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 10-11, 15-20 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No 6,401,200 by Nishiike et al in view of US Patent No 5,655,079 by Hirasawa et al.

In claim 1, Nishiike teaches about a method for down-loading data from an upper processor "Controller" to a plurality of lower processors "DSPs" of a mobile communications switching system in a process of resetting the processors, the method comprising (Col 1, lines 5-15) (Fig 3):

requesting an information download from the lower processors to the upper processor (Col 1, lines 5-15); (Boot process initiated by DSPs)

accessing a memory of the upper processor "master ROM" containing the requested information download (Col 4, lines 20-30);

grouping the lower processors with a representative address "Common boot address" (Col 2, lines 55-67) (Fig 4);

but does not explicitly teach about determining whether the accessed information has an error nor the IPC format as disclosed by applicant; and

Hirasawa teaches about creating the accessed information in an information processing code IPC format (Fig 7) (Col 4, lines 50-65);

determining whether the accessed information has an error (Col 10, lines 55-65);

transferring the IPC format information from the upper processor to the lower by using the group representative address, the transferred IPC format information including the accessed information and the group representative address (Col 7, lines 35-50) (Col 16, lines 10-20).

Hirasawa method provided an improvement approach to the downloading of code, which allowed one format to be used for group and individual download which reduces network traffic (Col 1, lines 35-45) (Col 2, lines 30-35).

It would have been obvious at the time of the invention for some one of ordinary skill to improve on the efficiency of Nishiike invention by utilizing Hirasawa's method, which reduces the amount of network traffic that is needed when configuring similar devices.

In claim 2, Nishiike combined with Hirasawa, teaches about a method of claim 1, wherein the resetting of the processors includes an initial loading and a re-loading (Nishiike Col 5, lines 30-40).

In claim 3, Nishiike combined with Hirasawa, teaches about a method of claim 1, wherein the group representative address includes all the lower processors (Fig 4)

In claim 4, Nishiike combined with Hirasawa, teaches about a method of claim 1, wherein the grouping the lower processors comprises grouping the plurality of lower processors using the group representative
address "Common boot address" (Fig 4).

In claim 5, Nishiike combined with Hirasawa, teaches about a method of claim 1, wherein the grouping the lower processors comprises grouping at least one additional lower processor (Fig 4).

In claim 10, Nishiike combined with Hirasawa, teaches about a method for downloading data from a first processor "Controller" to a plurality of second processors "DSPs" while resetting the processors, the method comprising (Nishiike Col 1, lines 5-15) (Fig 3):

transmitting a request for an information download from the plurality of second processors to the first processor (Nishiike Col 1, lines 5-15); (Boot process initiated by DSPs)

accessing a memory once of the first processor for the requested information (Nishiike Col 4, lines 35-40);

grouping the second processors using a prescribed processor address (Nishiike Col 4, lines 20-30); and

assembling the accessed information in a prescribed format (Covered in claim 1) ; and

transferring the assembled requested information from the first processor to at least two second processors using a group representative address, the transferred assembled request information including the accessed information and the group representative address (Covered in claim 1).

In claim 11, Nishiike combined with Hirasawa, teaches about a method of claim 10, wherein the grouping of the plurality of lower processors is performed using the group representative address (Fig 4).

In claim 15, Nishiike combined with Hirasawa, teaches about a method of claim 10, wherein the method further comprises determining whether the accessed requested information has an error (Hirasawa Col 10, lines 55-65).

In claim 16, Nishiike combined with Hirasawa, teaches about a mobile communications switching method comprising (Fig 3):

requesting information from a first processor "Controller" (Nishiike Col 1, lines 5-15) (Fig 3);

grouping a plurality of second processors "DSPs" using a representative address of the plurality of second processors(Nishiike Col 1, lines 5-15) (Nishiike Col 2, lines 55-67);

providing the requested information in an information processing code (IPC) format (Covered in claim 1); and

transferring the requested information in the IPC format from the first processor to the plurality of second processors based on the representative address of the plurality of second

processors , the transferred information in the IPC format including the request information and the representative address of the plurality of the second processor (Fig 4) (Covered in claim 1).

In claim 17, Nishiike combined with Hirasawa, teaches about a method of claim 16, further comprising accessing a memory of the first processor having the requested information (Nishiike Col 5, lines 5-10) .

In claim 18, Nishiike combined with Hirasawa, teaches about a method of claim 17, further comprising determining whether the requested information has an error (Covered in claim 1).

In claim 19, Nishiike combined with Hirasawa, teaches about a method of claim 16, wherein the method is provided in a process of resetting the second processors (Nishiike Col 4, lines 40-50). (In order to prevent corruption of the configuration data, a boot process has to be preceded by a reset in this way the device will be placed in a known state prior to being boot)

In claim 20, Nishiike combined with Hirasawa, teaches about a method of claim 19, wherein the resetting of the second processors includes an initial loading and a re-loading (Nishiike Col 5, lines 30-40).

In claim 24-26, Nishiike combined with Hirasawa, teaches about a method wherein group representative address comprises an address of at least two of the lower processor (Hirasawa Col 4, lines 20-30) (Hirasawa Col 16, lines 10-20) (Covered in claim 1).

Allowable Subject Matter

1. Claims 6-9, 12-14, and 21-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. The following is a statement of reasons for the indication of allowable subject matter: prior art failed to teach about using a representative address that comprises a node address (NA), a BHIU address (BA), a cinu address (CA), and a slot address (SA).

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent 6,212,557 by Oran teaches about a method and apparatus for synchronizing upgrades in distributed network data processing systems.

US Patent 6,021,442 by Ramanan et al, teaches about a method and apparatus for partitioning an interconnection medium in a partitioned multiprocessor computer system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael S. A. Delgado whose telephone number is (571) 272-3926. The examiner can normally be reached on 7.30 AM - 5.30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on (571) 272-3923

. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MD

DAVID WILEY
SUPERVISORY PATENT EXAMINER
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